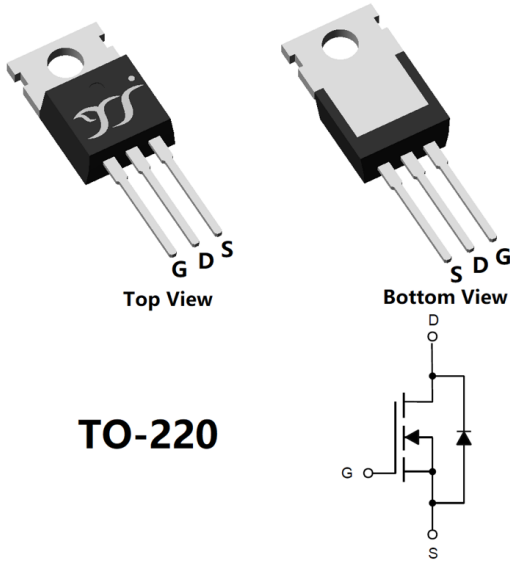


N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 100V
- I_D 190A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<3.1m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Load switch
- Battery management
- Solar

Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	100	V
Gate-source Voltage			V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	$T_A=25^\circ C, V_{GS}=10V$	I_D	-	24.1	A
		$T_A=100^\circ C, V_{GS}=10V$		-	17	
Continuous Drain Current (Note 1,3)	Steady-State	$T_C=25^\circ C, V_{GS}=10V, \text{Chip limitation}$		-	190	
		$T_C=100^\circ C, V_{GS}=10V$		-	134	
Pulsed Drain Current	$T_C=25^\circ C, t_p \leq 10\mu s$		I_{DM}	-	760	
Maximum Body-Diode Continuous Current	$T_C=25^\circ C$		I_S		175	
Avalanche Energy (non-repetitive)	$T_J=25^\circ C, V_G=10V, R_G=25\Omega, L=0.5mH, I_{AS}=50.3A$		EAS	-	632.52	mJ
Total Power Dissipation (Note 1,2)	Steady-State	$T_A=25^\circ C$	P_D	-	3.75	W
		$T_A=100^\circ C$		-	1.87	
Total Power Dissipation (Note 1,3)	Steady-State	$T_C=25^\circ C$		-	230	
		$T_C=100^\circ C$		-	115	
Junction and Storage Temperature Range			T_J, T_{STG}	-55	175	$^\circ C$

Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	40	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	0.65	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJP3D1G10H	B1	YJP3D1G10H	50	/	5000	Tube



YJP3D1G10H

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA, T _j =25°C	100	-	-	V
		V _{GS} =0V, I _D =1mA, T _j =25°C	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V, T _j =25°C	-	-	1	μA
		V _{DS} =100V, V _{GS} =0V, T _j =125°C	-	-	100	
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V, T _j =25°C	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA, T _j =25°C	2.1	2.9	3.7	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =50A, T _j =25°C	-	2.5	3.1	mΩ
Diode Forward Voltage	V _{SD}	I _S =50A, V _{GS} =0V, T _j =25°C	-	0.84	1.2	V
Gate Resistance	R _G	f=1MHz, T _j =25°C	-	2.3	-	Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=0.5MHz, T _j =25°C	-	7076	-	pF
Output Capacitance	C _{oss}		-	2348	-	
Reverse Transfer Capacitance	C _{rss}		-	42	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =50A, T _j =25°C	-	94	-	nC
Gate-Source Charge	Q _{gs}		-	30.5	-	
Gate-Drain Charge	Q _{gd}		-	15	-	
Reverse Recovery Charge	Q _{rr}	I _F =50A, di/dt=100A/μs, V _{GS} =0V, V _R =50V, T _j =25°C	-	50	-	nC
Reverse Recovery Time	t _{rr}		-	48	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DS} =50V, I _D =50A, R _L =1Ω, R _{GEN} =3Ω, T _j =25°C	-	29	-	ns
Turn-on Rise Time	t _r		-	54	-	
Turn-off Delay Time	t _{D(off)}		-	67	-	
Turn-off Fall Time	t _f		-	42	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of R_{θJA} is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with T_A=25°C. The maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad).



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Typical Electrical and Thermal Characteristics Diagrams

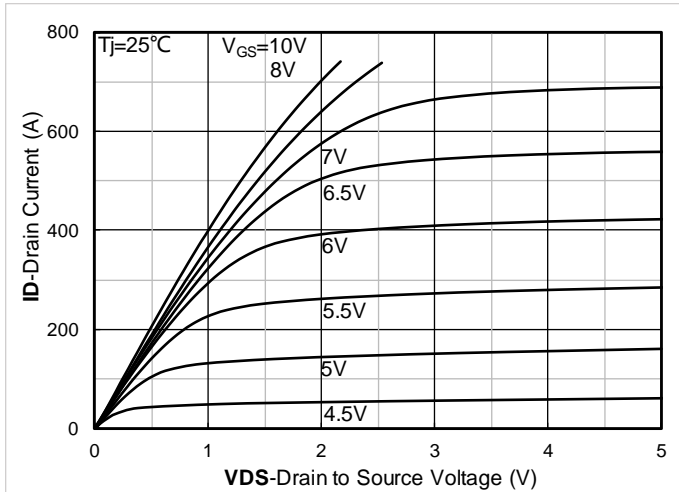


Figure 1. Output Characteristics; typical values

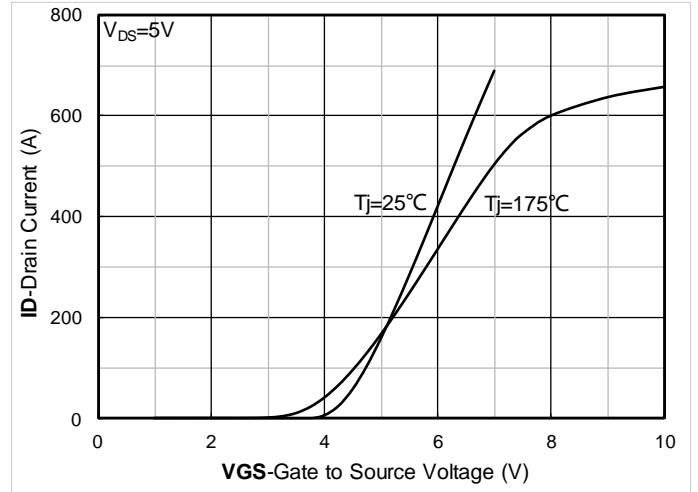


Figure 2. Transfer Characteristics; typical values

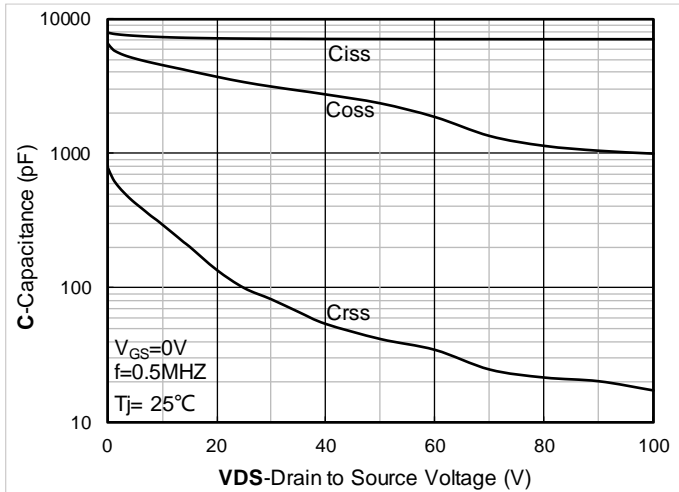


Figure 3. Capacitance Characteristics; typical values

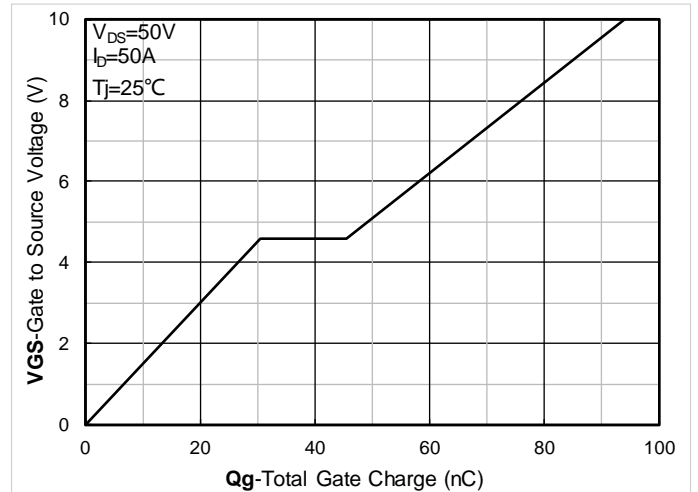


Figure 4. Gate Charge; typical values

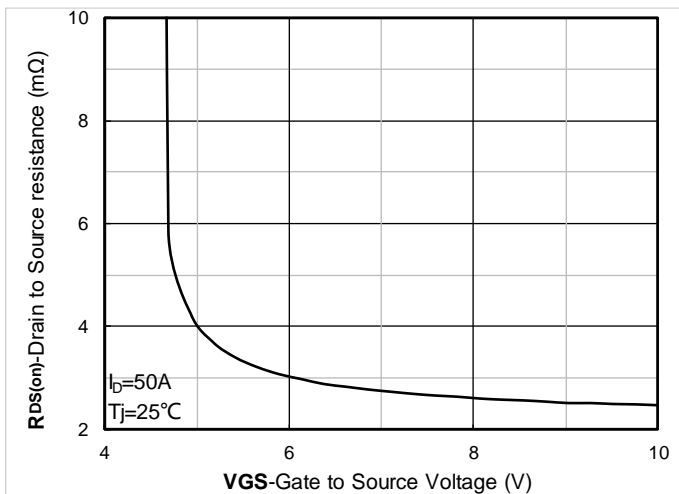


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

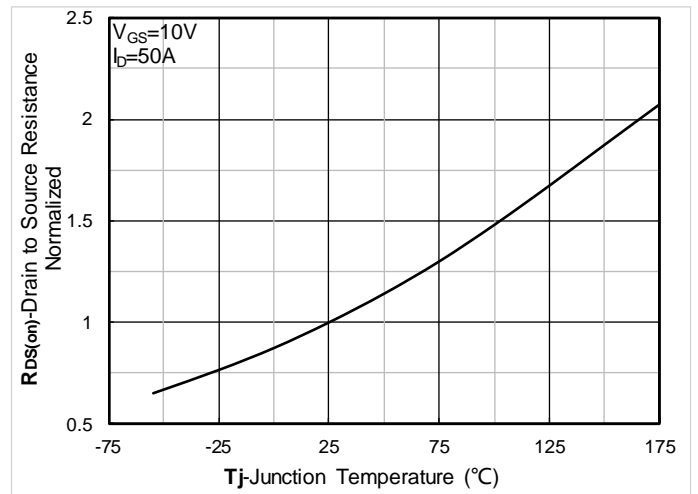


Figure 6. Normalized On-Resistance



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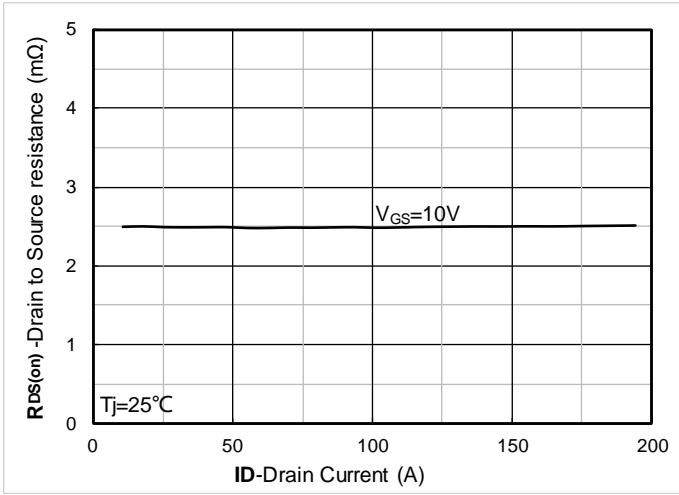


Figure 7. RDS(on) vs. Drain Current; typical values

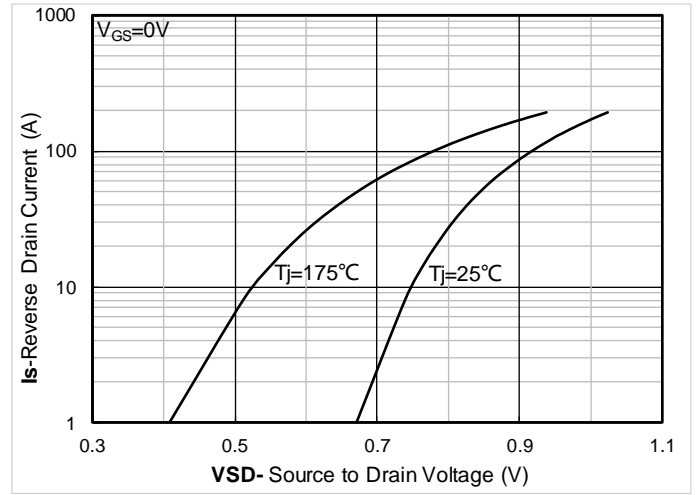


Figure 8. Forward characteristics of reverse diode; typical values

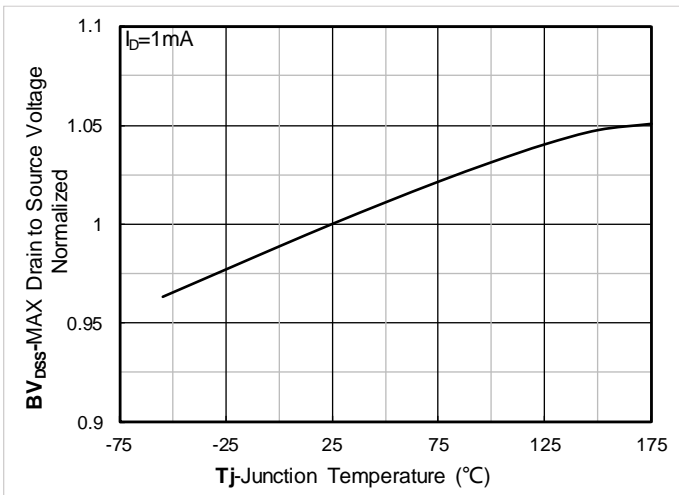


Figure 9. Normalized breakdown voltage

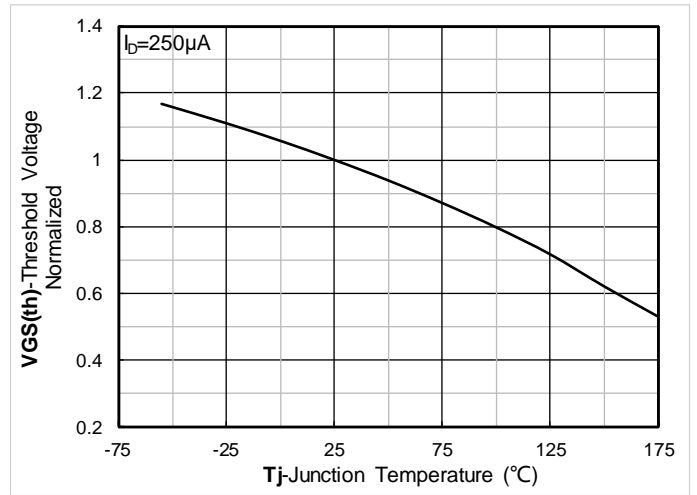


Figure 10. Normalized Threshold voltage

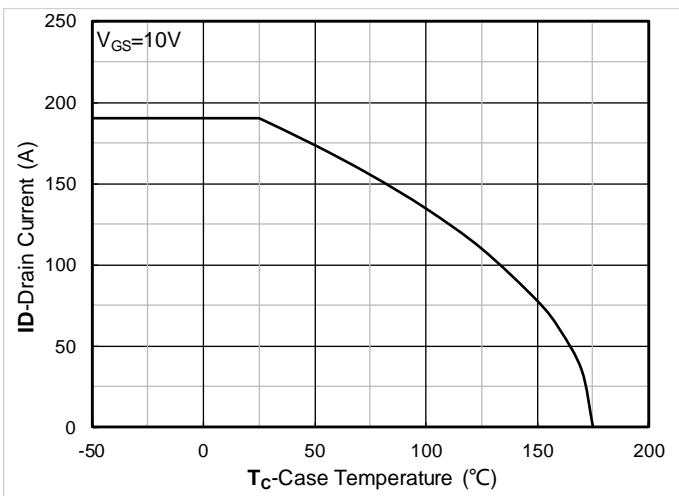


Figure 11. Current dissipation

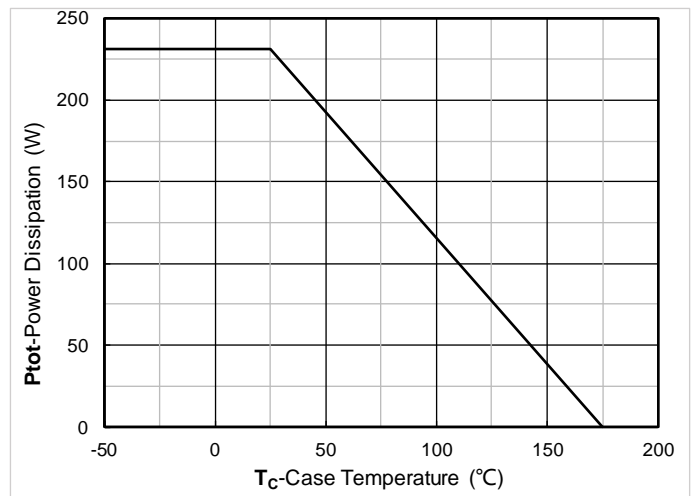


Figure 12. Power dissipation



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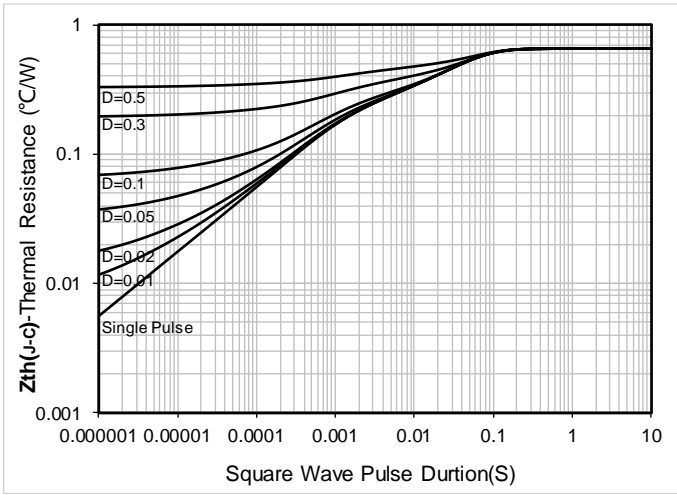


Figure 13. Maximum Transient Thermal Impedance

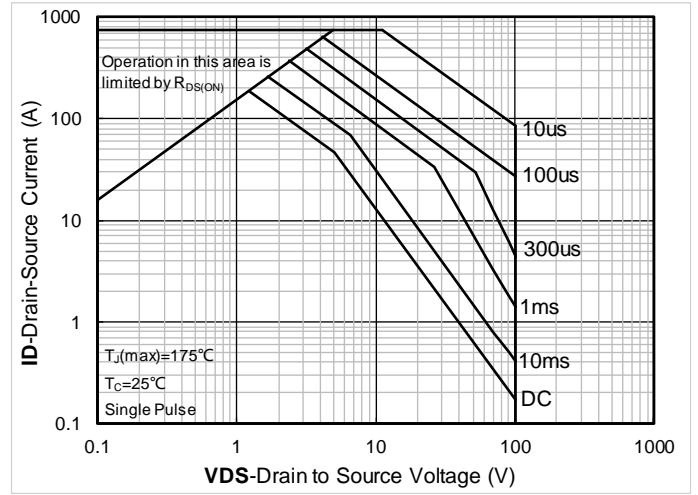


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

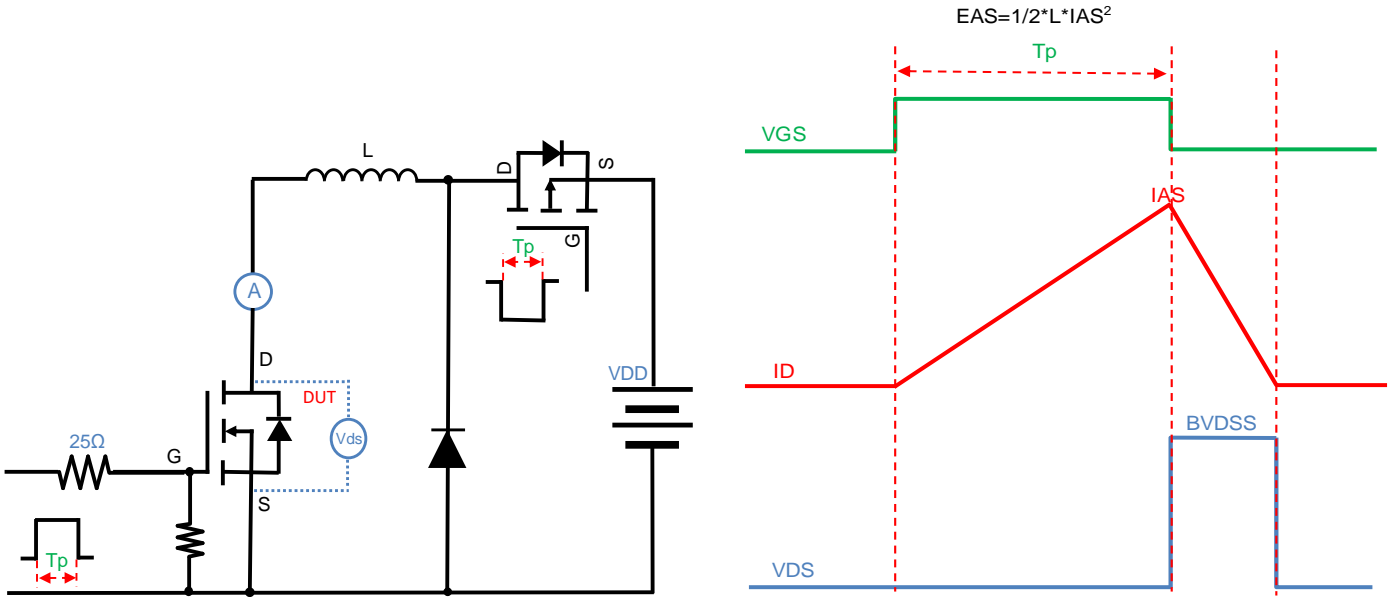


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

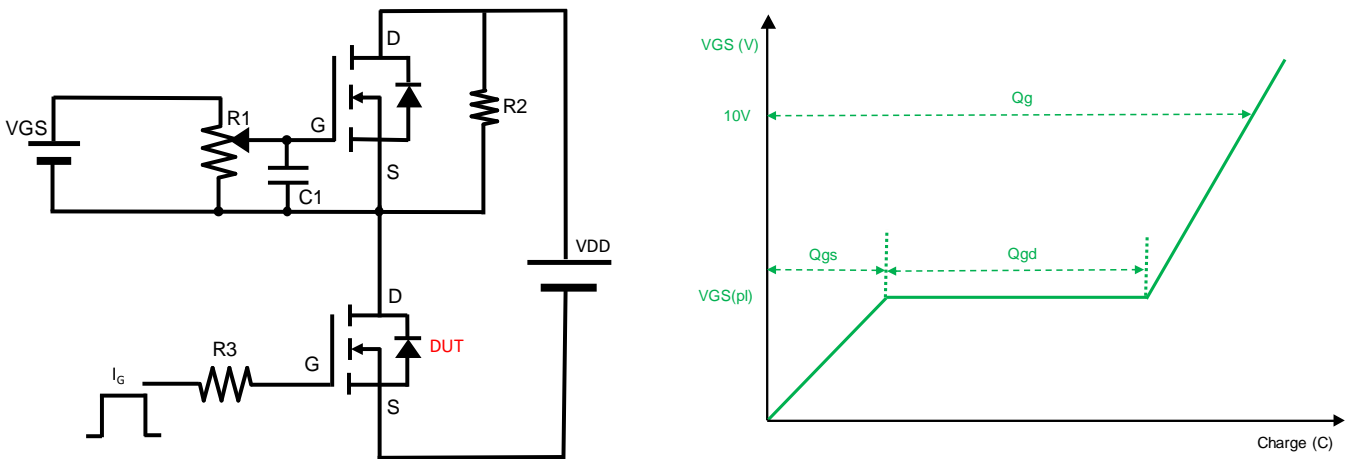


Figure B. Gate Charge Test Circuit & Waveform

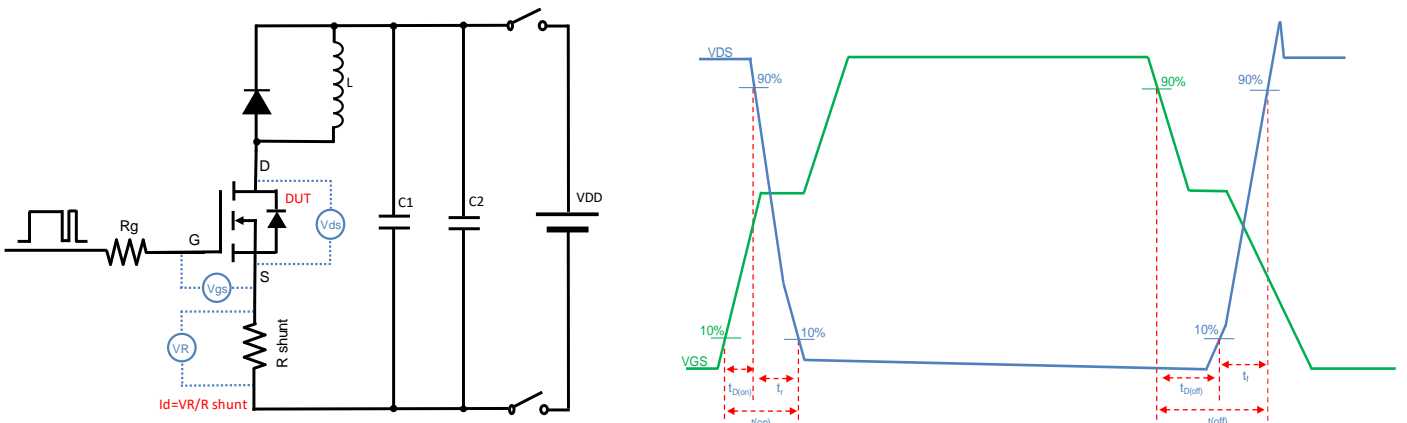


Figure C. Resistive Switching Test Circuit & Waveform

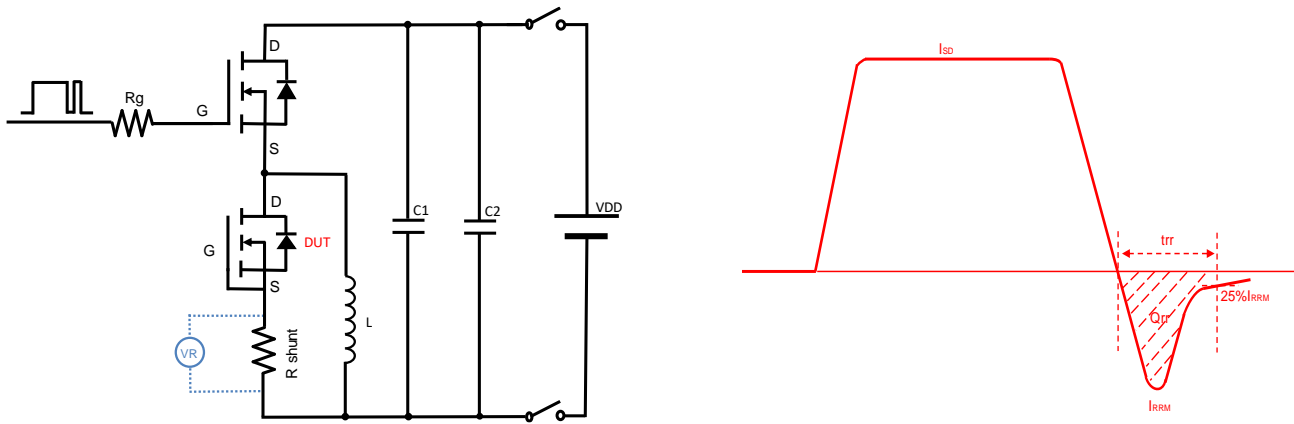
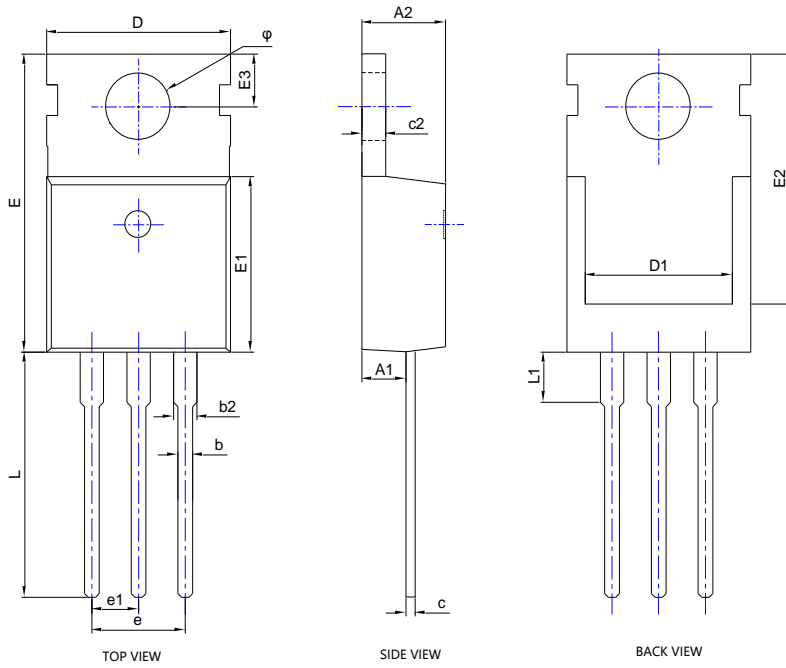


Figure D. Diode Recovery Test Circuit & Waveform



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TO-220AB-E Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A1	0.093	0.114	2.350	2.900
A2	0.176	0.184	4.470	4.670
b	0.028	0.036	0.710	0.910
b2	0.048	0.054	1.220	1.360
c	0.019	0.024	0.470	0.600
c2	0.047	0.055	1.200	1.400
D	0.382	0.408	9.700	10.370
D1	0.276	0.350	7.000	8.890
E	0.579	0.622	14.700	15.800
E1	0.350	0.373	8.900	9.470
E2	0.463	0.535	11.750	13.600
E3	0.108BSC		2.740BSC	
e	0.200BSC		5.080BSC	
e1	0.100BSC		2.540BSC	
L	0.508	0.583	12.900	14.800
L1	0.100	0.151	2.540	3.840
φ	0.142	0.154	3.600	3.900

NOTE:
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.



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